

In the Drawings:

The attached drawing sheet includes changes to Fig. 19. The annotated sheet showing the change is attached. The replacement sheet contains the words “Prior Art” and replaces the originally filed sheet.

## **REMARKS**

Fig. 19 and the title have been amended as required.

Claim 1 has been amended to overcome the outstanding § 112 rejection, by defining “ICs” as “integrated circuits.” This term and its association with its abbreviation (ICs) is well understood in the art, as the examiner recognizes. Withdrawal is requested.

The § 112 rejection of claim 4 has been overcome by amending claim 4 without narrowing the scope of the claim. Withdrawal is requested.

Claims 7, 9, 10 and 11 stand rejected under § 102 on the basis of Go ‘566. Applicant traverses the rejection of claims 7 and 10 because the cited reference does not disclose (or suggest) the selection of a first or second clock signal based on a selection signal, as in amended claims 7 and 10.

Claims 7 and 10 now recite that the data driver IC inputs a selection signal and selects the first or second clock signal based on the selection signal. This feature is supported by page 22, lines 8-11 and 18-21 of the present Specification and Fig. 18.

Go ‘566 fails to disclose (or suggest) this feature of claims 7 and 10. As shown in Fig. 10 of Go ‘566, a data driver IC 120 does not input a selection signal and does not select the first or second clock signal FD 1, FD2 based on the selection signal.

Claim 9 recites a first data latch that inputs a first clock signal and latches data signals of odd-number dots with the first clock signal, and a second data latch that inputs a second clock signal in reverse relation with the first clock signal and latches data signals of even-number dots with the second clock signal. This feature is supported by page 18, lines 12-18 of the present Specification and Figs. 11-13.

In contrast, Go'566 discloses a latch 200 (see Figs. 10 and 12). However, a data driver IC 120 has only one latch 200 and does not have two latches. Furthermore, although first and second clock signals FD1 and FD2 are input to data lines D1-D6 through a respective XOR gate (160 or 210), the latch 200 does not input the first and second clock signals FD1 and FD2 (see Abstract, Figs. 10 and 12). Therefore, Go '566 fails to disclose or suggest this feature of claim 9.

Claim 11 recites that a timing controller displaces the phase between data signals of odd-number dots and even-number dots on the same horizontal line by 180 degrees.

In contrast, Go '566 discloses that the data driver IC 120 displaces the phase between first video signals S'1, S'3 and S'5 of the odd data lines D1, D3, and D5 and second video signals S'2, S'4 and S'6 of the even data lines D2, D4, and D6 by 180 degrees (see column 6, lines 23-27, Figs. 10-12). However, Go '566 fails to disclose or suggest this feature of claim 11. Accordingly, withdrawal of this rejection is requested.

Claims 1 and 5 stand rejected under § 103 on the basis of Go '566 and Misawa et al. '936. Applicant traverses this rejection because the cited references do not disclose or suggest a second clock signal line in parallel with a first signal line, or the load means recited in independent claim 1.

Claim 1 recites, among other things, that a second clock signal line is equipped in parallel with the first signal line. In contrast, Misawa '936 teaches that a CL line 218 and an inverted CL line 219 are twisted, crossing near their centers 220 (see col. 12, lines 31-32 and FIG. 11A). Accordingly, the inverted CL line 219 of Misawa '936 is not configured in parallel with the CL line 218. Therefore, if the CL line 218 and inverted CL line 219 of Misawa '936

were incorporated to Go '566, a first clock signal line and second clock signal line of Go '566 would be twisted, crossing, and thus, would not be arranged in parallel with each other. Therefore, Misawa '936 teaches away from the combination of Go '566 and Misawa '936.

Furthermore, the examiner recognizes that Go '566 does not teach the load means of claim 1 (paragraph 16). The examiner argues that Misawa '936 discloses the claimed load means, but applicant respectfully disagrees.

As described in column 12, lines 25-39, Misawa '936 tries to cancel stray capacitance by locating its clock lines an equal distance from a video signal bus. Of course, there is no assurance that the stray capacitance will actually be cancelled, and there is no way to make the load capacitances balanced. For these reasons, Misawa '936 does not disclose the claimed load means of claim 1.

The load means of the present invention is a structural element which can take many forms, such as the load terminals recited in claim 2, or the capacitor recited in claim 3. The load means compensates for capacitance differences which result from the layout of lines, for example. In other words, the layout of lines in Misawa '936 is not the load means of the present invention.

In paragraph 18 of the office action, the examiner argues that the motivation for combining the references is the "consistently progressive goals" of reducing noise and improving picture quality. This is insufficient to show motivation, because it does not show a motivation to address noise and picture quality in the manner of the present invention. In other words, there is no motivation to combine Go '566 with Misawa '936, and then add the parallel signal lines and load means of the present invention. Accordingly, withdrawal of this rejection of claim 1 and dependent claim 5 is respectfully requested.

The rejections of dependent claims 2, 3 and 4 (paragraphs 20-28) are traversed for the reasons given for claim 1.

Claim 6 stands rejected under § 103 on the basis of Go '566, Misawa '936 and Ogata JP '337. In addition, claims 8 and 12 stand rejected under § 103 on the basis of 'Go 566 and Ogata. Applicant traverses these rejections for the following reasons.

Claims 6, 8 and 12 recite that a data signal of a dot consists of a plurality of bits (a first feature). Claims 6, 8 and 12 also recite that each bit of an odd-number dot and the same bit of an even-number dot are adjacent to each other (a second feature).

In contrast, Ogata discloses that a data signal of a bit (which corresponds to the "dot" of claims 6, 8 and 12) consists of one bit (see Fig. 1). Therefore, Ogata fails to disclose or suggest the first feature of claims 6, 8 and 12. Furthermore, since Ogata fails to disclose that a data signal of a dot is consisted of a plurality of bits, Ogata fails to disclose or suggest the second feature of claims 6, 8 and 12. Go '566 and Misawa '936 also fail to disclose or suggest the first and second features of claims 6, 8 and 12. Withdrawal of these rejections is requested.

For the foregoing reasons, applicant believes that this case is in condition for allowance, which is respectfully requested. The examiner should call applicant's attorney if an interview would expedite prosecution.

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